Development of a Capacity Planning Simulation Model for Semiconductor Wafer Fabrication

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Abstract. Semiconductor wafer fabrication is a capital intensive industry, how to effectively utilize the capacity is always a crucial challenge for semiconductor capacity planners. Currently, static capacity planning model, which is based on the historical data of the average available time of machines and routing, is usually employed to plan the required capacity for satisfying the demand plan. Due to the complexity of semiconductor production and many production constraints (e.g., re-entry, batching) and abnormal events (e.g., machine breakdown) are not considered, the static model is very hard to estimate a reasonable capacity plan for satisfying a weekly/monthly demand (i.e., wafer out) plan. Therefore, this paper aims to develop a capacity planning and analysis simulation (CPAS) system which takes into account the production characteristics/constraints, the internal behavior of machines, and the dispatching rules applied in a full-scale 300 mm wafer fab. Rapid application development (RAD) and unified modeling language (UML) are employed to analyze and designed CPAS, and a commercial available simulation software, *Plant Simulation*, is used to implement CPAS. The accuracy of the CPAS model is validated with the actual input (e.g., wafer release per day, machine run time/available time, routing, WIP) and output (e.g., cycle time, MOVE, Wafer Out) for all machine tool sets. The CPAS model was also employed by capacity planners in a leading wafer fab in Taiwan to study the effect of the fluctuation of available time (AT) of critical/bottleneck production equipment to fab' s overall capacity and output performance.

Keywords: Semiconductor Manufacturing, Simulation System Development, Capacity Planning, Unified Modeling Language (UML)

1. INTRODUCTION

The semiconductor industry in Taiwan has demonstrated astonishing growth and become one of the major IC producers in the world, especially in " Wafer Fabrication". TSMC today announced that the Company earned the highest ranking for the Semiconductor Manufacturing Sector. The market share in TSMC increases from 47 in 2013 to 53 percent in 2014. The total production value of Taiwan's semiconductor industry reached NT$1.895 trillion in 2014, and 7.8 percent growth rate. Thus, the semiconductor is the quite important industry for the domestic economy.

Currently, static capacity planning model, which is usually based on the historical data of the average available time of machines and routing, is usually employed to plan the required capacity for satisfying the weekly/monthly demand (i.e., wafer out) plan. The approach may employ heuristics, mathematical programming, local searching algorithm, artificial intelligence. Due to the capacity variation, the complexity of semiconductor production and many production constraints and frequently occurred abnormal events (e.g., machine breakdown) are not considered, the *planned capacity* determined by the static capacity planning model usually exceeds the *actual capacity*, and this gap represents the extra

production cost which will reduce the estimated profit. For instance, Fig 1 shows that the estimated unit cost per wafer of a 20K fab employing ideal planned capacity (the bottom curve) is much lower than actual capacity (the top curve). Essentially, fab management staffs believe that actual capacity curve is reasonable and ideal planned capacity is too optimistic and unachievable. On the contrary, capacity planners think that the performance of *actual capacity curve* is unreasonable even some unexpected abnormal events occurred. Therefore, capacity planners should plan capacity based on reasonable capacity (the middle curve) by considering the machine available time (AT), the fluctuation of AT and some unavoidable abnormal events (e.g., machine breakdown). It is obvious that the *reasonable capacity* cannot be obtained unless the capacity impact of machine AT and its fluctuation may be evaluated and accepted by fab management.

Because of the insufficient capacity, the impact of the capacity fluctuation of a machine to the overall fab's throughput may not be obvious. However, the level of stability and availability of critical machines may significantly affect the throughput performance when in the high season (i.e., demand may be larger than capacity). In other words, the static model may overestimate the capacity performance, which will result in the actual production cost exceeds the planned ideal cost, and leads to an inappropriate capacity investment decision.

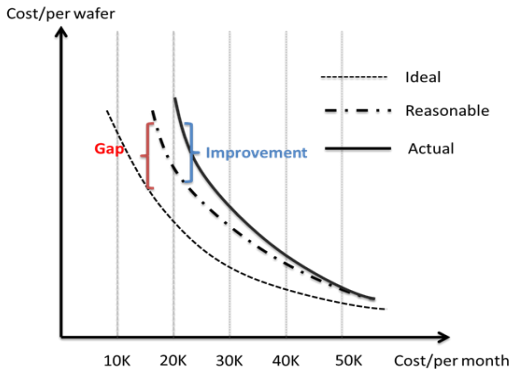

Figure 1: The caption of a figure should appear at the bottom of the figure.

To overcome the aforementioned drawbacks of a static model, dynamic capacity planning model is an appropriate approach in which simulation is widely applied. Thus, Bahaji and Kuhl (2008) developed a semiconductor production simulation model and employed design of experiment (DOE) and statistical analysis to evaluate fab performance by considering different ordering strategy and dispatching rules. Liu et al.(2011) developed a three phased multi-dimension model combining queuing model and simulation to study capacity planning and expansion problem by considering cycle time, throughput and product mix. Negahban and Smith [4] classified the research on the application of simulation in semiconductor may be classified into two categories: production equipment centered and non-production equipment (e.g., automated material handling system) centered. Although some research covers the entire Fab production equipment, only simple dispatching rules and production data (e.g., batch size, process time, routing) are considered.

In practice, the instability of machine tool's available time (AT) may dramatically cause fab's overall capacity/throughput loss, however, it is difficult to know the impact of the fluctuation of each machine's available capacity (i.e., AT%) under different product mix and production environment. On the contrary, if the level of impact may be obtained, shop floor man-agers only need to watch attentively on the "key" ma-chine tools, which will cause high impact on the throughput, and keep their promised AT level or in-crease AT level.

Furthermore, AT level of a machine tool will be affected by some unexpected factors (e.g., breakdown) or expected/controllable factors (e.g., preventive maintenance), capacity planners may schedule preventive maintenance at some appropriate time period if the impact of the pattern of AT fluctuation to the overall throughput (i.e., wafer out) may be obtained. Nazzal et al. developed a fab production simulation model, which considers simple dispatching rules and basic machine production data, and employs statistical analysis approach to identify the critical machine tool groups which heavily affect the capacity performance and throughput, then, supports a company's capacity expansion and in-vestment decision. However, existing research does not study the impact of operation characteristics or production constraints (e.g., the level of available time, breakdown, and maintenance) of critical machine tool groups to the throughput. Neither of existing research generates appropriate preventive maintenance (PM) schedule to fully utilize the available capacity as we proposed in this research.

Therefore, this paper aims to develop a capacity planning and analysis simulation (CPAS)model which takes into account the production characteristics /constraints, the internal behavior of machines, and the dispatching rules applied in a full scale 300 mm wafer fab. The CPAS model will also be applied in a leading wafer fab in Taiwan to study the impact of the available time (AT) and its fluctuation of critical/bottleneck production equipment to fab's overall capacity and output performance. A suitable capacity plan may therefore be made in order to effectively satisfy the weekly and monthly demand plan with the low cost and controllable cycle time.

The rest of the paper is organized as follows. Section 2 describes the characteristics of wafer fabrication process and current empirical approach for capacity planning. The application of CPAS model in a full-scale 300 mm wafer fab for capacity impact analysis (CIA) and capacity planning are described in Section 3. Finally, conclusions are presented.

2. BACKGROUND

2.1 Characteristics of wafer fabrication process

The semiconductor manufacturing process is composed of four main stage : IC design, IC manufacturing, assembly and final testing. Among the process, wafer fabrication due to its complex and re-entrant process. The longer period needed due to wafer process required 600 to 700 steps. Despite the complexity of wafer process, it need high quality of manufacturing. To assure the quality of every step of process, it has a testing in every end of steps as far as possible. This research focuses on wafer fabrication to develop system and we will describe detail wafer process step in this chapter.

A wafer starts from a cleaning operation, then, the wafer is moved to the furnace for the oxidation operation, followed by the deposition process by employing chemical vapor deposition (CVP) approach. Then, a lithography process starts by first paving a layer of photo resist, then, transferring mask pattern on the photo resist. The etching process will remove silicon nitride layer which is not protected and leave the required circuit diagram. Then, ion implantation process will proceed by implanting phosphorus atoms to the wafer and removing the photoresist.

It has furnace, photo-track, photo-exposure process, etching process, implanter, thin film process and measure in wafer fabrication in Fig2. The wafer circuit is made from thin film process, photo-exposure, etching process, etc and formed layer by layer. When a layer is completed, stacked layers and the amount of process will accumulate .

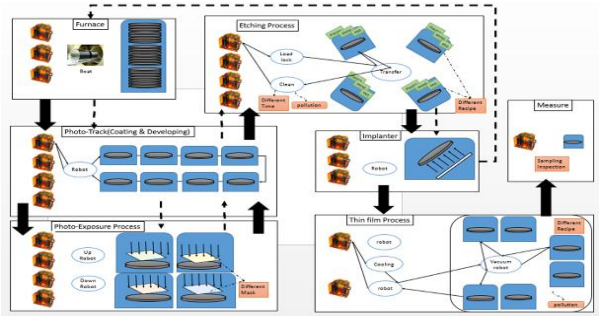

Figure 2: The basic operations of wafer fabrication.

In order to study the capacity impact of machine available time (AT) and its fluctuation, the machine tools may be classified as four types: (1) single chamber machine (SCM), (2) multi-chamber machine (MCM), (3) continuous chemical machine (CCM), and (4) batching machine (BM). SCM needs to consider upload/download and process times, MCM needs to consider which chamber is occupied and each chamber's different down time in addition to upload/download and process times. For CCM, the download time is the upload time plus process time, and BM needs to include waiting time till the batch size is reached and begin processing (Fig. 3a). For machines in different manufacturing processes, the following characteristics need to be considered (Fig. 3b):

(1) Priority – each wafer lot has its production priority, such as normal lot, engineering lot, hot lot, and super hot lot, machine tool (e.g., Photo Lithography) will select lot based its priority.

(2) Queue time – some manufacturing processes (e.g., Thin-Film) have time constraints, such as it needs to rework or become scrap if the cycle time or the time between two operations exceed a specific time period.

(3) Recipe/Mask – every chamber of multi-chamber machines (e.g., Exposure, Etch) with specific recipe/machine can different technologies.

(4) Pollution (metal) flag – a flag is marked for machine tool, such as Etching, whose manufacturing process has metal contamination, the remaining lots waiting in the buffer of the machine tool need to be transferred to other machine tools if it exceeds its pre-determined daily upper limit.

(5) Batching – many machine tools (e.g., Diffusion) with multi-chambers, need to process lots with batch size requirement in order to avoid capacity waste.

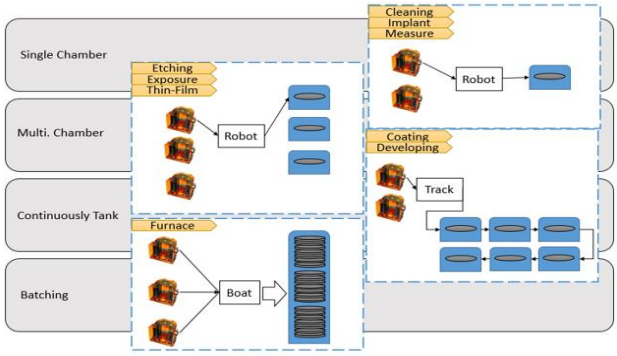

Figure 3a: Classification of machine tools

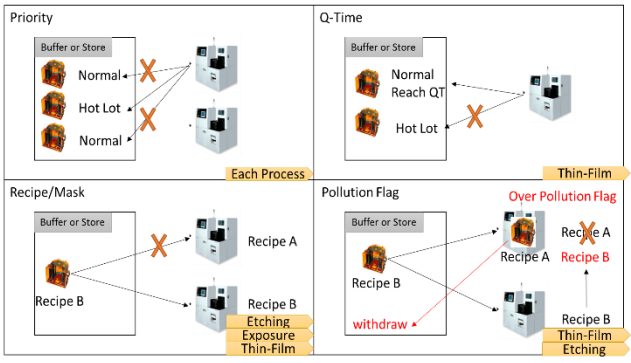

Figure 3b: Classification of machine tools

As we notice from Fig. 3, many machine tools in deposition, lithography, etching and ion implantation processes have multi-chamber operations characteristics whose available time (AT) and its fluctuation usually will significantly affect the throughput of wafer fab, however, it is difficult to generate an effective capacity plan and capacity impact analysis report unless the internal behavior of these machine tools are modeled. Generally, a multi-chamber machine can be classified as a parallel machines which simultaneously process several equivalent or distinct operation processes. In wafer fab, distinct chambers can have different recipes and masks for specific product (i.e., technology) and its corresponding manufacturing process. Let's take the metal etch systems used in aluminum metal etch process as an example, it has three load ports, two load lock (e.g., A, B), one robotic arm loading/unloading wafer between load port and load lock, one mechanical carrousel, and four chambers (e.g., 1 to 6) stored with different recipes, the machine can simultaneously process two different technologies whose routes will be load port-A-2-1-A-load port and load port-B-3-4-B-load port, hence, the capacity of this multi-chamber metal etch machine can be counted as two single-chamber machines (see Fig . 4).

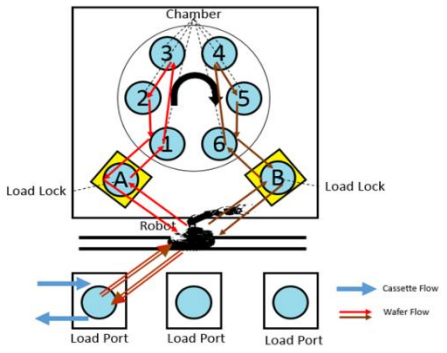

Figure 4: The operations of a multi-chamber machine.

2.2 Empirical approach for capacity planning

The current industry heuristic capacity planning involves four steps: (1) Determining the daily wafer out based on projected wafer demand, (2) Determining the average daily available machine numbers, (3) Calculating the average daily required machine time for satisfying the daily demand according to technology routing and processing time, (4) Calculating the aver-age daily loading percentage of each machine. For example, an order request for 300 wafer A and 240 wafer B, there are 10 machines available, the average available time (AT) is 97%, the testing equipment is 1%, machine efficiency is 98% and batching percentage is 84%. Processing time of wafer A is 0.03 hour, processing times of wafer B's first (B-1) and second (B-2) process are 0.02 and 0.06 hours, respectively. Then, capacity planners can calculate the average daily loading of each machine shown as follows.

Step 1: The daily wafer out of A is 10 (=300/30) and B is 8 (=240/30)

Step 2: The average daily available machine number is 7.9027 (= 10x(0.97-0.01)x0.98x0.84)

Step 3: The average daily required machine time is 0.94 hours since the average daily required machine time of wafer A and B are 0.3 (= 10x0.03) and 0.64 (=8x0.02+80x0.06) hours, respectively.

Step 4: The average daily loading of each machine is 0.12 (= 0.94/7.9027).

Since heuristic capacity planning approach is usually based on the historical data of the average available time of machines and routing, the production constraints (e.g., Qtime, batching), machine characteristics (e.g., multi-chamber), dispatching rules and frequently occurred abnormal events (e.g., machine breakdown) are not considered, it is very hard to generate a reasonable capacity plan for satisfying a weekly/monthly demand (i.e., wafer out) plan. Furthermore, it cannot be applied to study the impact of machine available time (AT) and AT fluctuation to fab's capacity and throughput performance (e.g., WIP, wafer out), which will result in the actual production cost exceeds the planned ideal cost, and leads to an inappropriate capacity investment decision.

3. CAPACITY ANALYSIS & PLANNING SIMULATION SYSTEM

3.1 The proposed system framework

In order to estimate the reasonable fab capacity and effectively utilize the capacity, the CPAS model should have the capability of simulating the entire wafer fabrication process in a full-scale 300 mm wafer fab, accurately evaluating and effectively planning a semiconductor fab's capacity, clustering and identifying key machine tools potentially with high capacity impact so that fab managers and capacity planners can put more attention on them. Therefore, the main characteristics/functions of the proposed CPAS system may be summarized as follows.

(1) Timely and accurately simulate the released order's lot/wafer fabrication process: CPAS model can timely and accurately model the fabrication process of each lot/wafer and the performance of each machine tool (e.g., WIP, moves, utilization) by taking into account the production characteristics/constraints (e.g., Qtime, batching), the internal behavior of machines, the dispatching rules, and the abnormal events (e.g., machine breakdown) in a real wafer fab.

(2) Effectively evaluate and plan a semiconductor fab's

capacity: CPAS model can effectively generate accountable production schedule, based on the accepted combinatorial dispatching rules, to satisfy a weekly/monthly demand (i.e., wafer out) plan in terms of certain objectives (e.g., high utilization, short cycle time, less WIP).

(3) High capacity impact analysis: CPAS model can help capacity planners to study the impact of operation characteristics or production constraints (e.g., the level of machine tool available time, breakdown, maintenance) of critical ma-chine tool groups to fab's capacity and through-put performance (e.g., WIP, wafer out) under different product mix and production environment, and find out a cost effective capacity plan (e.g., outsourcing or renting extra machines), to avoid a capacity loss and inappropriate capacity investment decision.

In order to fulfill the aforementioned characteristics, Fig. 5 depicts the framework of a CPAS which is com-posed of five major modules: (1) input, (2) simulation, (3) capacity planning, (4) capacity impact analysis (CIA), and (5) output. The proposed CPAS can also integrate with external information application systems (e.g., ERP and MES) to respond to the external changing environment. The role and functions of each module are briefly described as follows.

(1) Input module
Input module is composed of data files and logic files, the material related data (e.g., MO, product technology, routing) imported from ERP, and machine tool related data (e.g., machine tool available time, runtime, recipe, scheduled PM) comes from MES. Logic files store the production constraints (e.g., QTime, machine metal flag) and dispatching rules (e.g., batching, priority) frequently applied in semiconductor fabs

(2) Simulation module
Simulation module, the core of CPAS system, is composed of simulation engine, simulation rule controller, and simulation parameter controller. Based on the released manufacturing order (MO) and fab's production characteristics, constraints and dispatching rules, simulation module will timely and accurately mimic the fabrication process of each lot/wafer and the performance of each machine tool (e.g., WIP, moves, utilization) in the wafer fab.

(3) Capacity planning (CP) module
Capacity planning module mainly provides an interface for users to set planning and control parameters of Simulation module, select the planned and released manufacturing orders (MOs) from ERP, import the timely and active fab production information and events provided by MES. Then, CP module will activate Simulation module to generate accountable production/operations schedule which usually fully utilizes available capacity to satisfy a weekly/monthly demand (i.e., wafer out) plan.

(4) Capacity impact analysis (CIA) module
Based on the studied production environment (e.g., a machine tool group is maintained at a certain AT level) and simulation results, CIA may employ K-means clustering technique and Kruskal-Wallis test (i.e., K-W test) to study the impact of the available time (AT) and AT's fluctuation of critical/bottleneck machine tool group to fab's overall capacity and throughput performance (e.g., moves, wafer out).

(5) Output module
Two types of outputs are stored in the data base, one is production output performance (e.g., daily sum, cycle time, run sheet, WIP by flow, move by flow), the other is analysis result (e.g., key ma-chine tools, AT fluctuation impact, scheduled PM). All the production output information will be routinely (e.g., one day simulation results) ex-ported to external data bases through ODBC (Open Database Connectivity). Analysis results will be stored and manipulated in SQL, then analyzed and graphically represented using Excel.

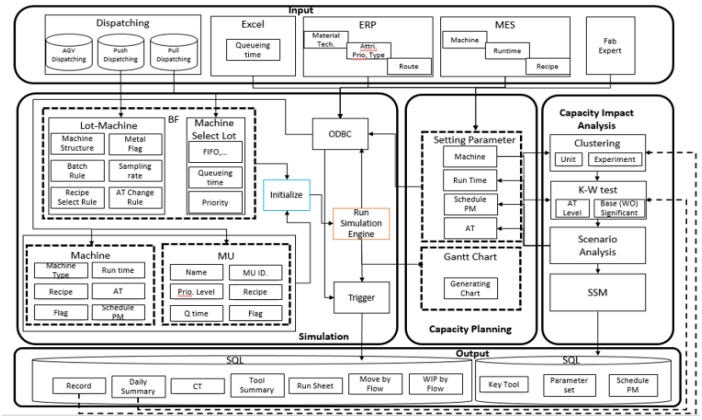

Figure 5: The framework of CPAS

3.2 Simulation modules in capacity analysis and planning simulation system

In order to develop a flexible and easy to maintain software model, we decide to develop an object-oriented capacity planning and analysis simulation model. The class diagram of CPAS, depicted in Fig. 6, is classified as five types: material flow, movable units, information flow, capacity planning, and capacity impact analysis. The characteristics and relationship of classes in CPAS class diagram are briefly described as follows.

- Material flow (MF): Classes Source, Buffer, Store and Plants/Machines belong to this category, a machine has sub-classes Load_Port, Chamber (single, multiple), and Load-Lock. Class Buffer includes Lot-select-Machine (LsM) dispatching method and attributes of machine

constraints, machine available time (AT), metal flag, batching rule, machine operation formula (i.e., recipe). Class Store includes Machine-select-Lot (MsL) dispatching method which considers FIFO, Priority, QTime.

- Movable units (MU): Classes Entity, Container, and Transporter belong to this category, wafer and cassette are the objects of Entity and Container, respectively.
- Information flow (IF): Classes Initialize, Trigger for simulation events triggering, ODBC, and Table File belong to this category.
- Capacity planning (CP): this class includes Set-ting Parameter and Gantt Chart sub-classes. Simulation parameters mainly include material information (e.g., product technology, routing, type, production queue time limitation, priority) and machine tool information (e.g., processing time, yield rate, recipe, breakdown rate, maintenance/repair time, operation behavior).
- Capacity impact analysis (CIA): this class includes Clustering, K-W test and Scenario Analysis sub-classes.

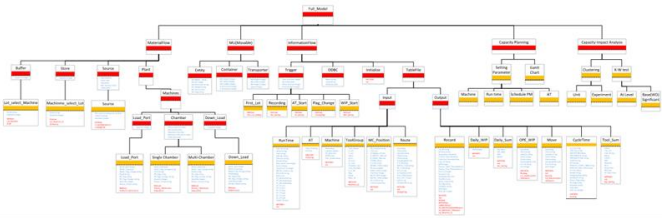

Figure 6: The class diagram of CPAS

We can further demonstrate the message passing among the classes and the system operation process of capacity planning, depicted in Fig. 7, may be represented using UML's sequence diagram, each class's method and the information passing among the related classes are briefly described as follows.

Step 1: Initialize the simulation model, including the machine, buffer, store and WIP.

Step 2: Start Simulation, check MU's route to find out next process's buffer and move to buffer.

Step 3: Call Lot-select-Machine dispatching method based on process type (e.g., regular or measuring ma-chine).

Step 4: Check machine status (e.g., capacity, pollution flag, recipe), move MU to store if machine Status is failure or with different flag. Then, record MU information in store WIP table. Go to Step 6.

Step 5: If machine status is standby, move MU into machine and start processing and record MU process information in run sheet.

Step 6: When MU's operation process complete, call Machine-select-Lot dispatching method based on dis-patching rules (e.g., FIFS, SPT, critical ratio)

Step 7: Check MU Info in store WIP table and select a lot to process.

Step 8: Move selected lot to move-into-machine and start operation process.

Step 9: Repeat Steps 2-8 till all the lots are processed.

Step10: Export simulation data

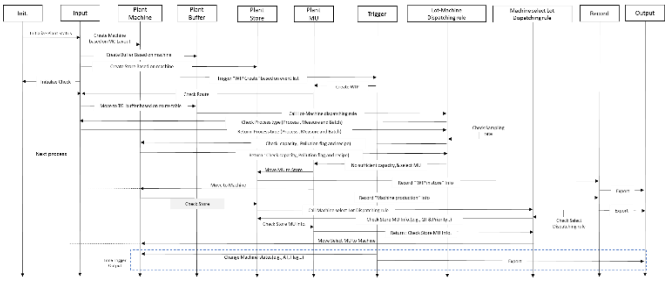

Figure 7: The system operation process of CP module Capacity Impact Analysis.

3.3 Implementation of capacity analysis and planning simulation system

In this research, a commercial object-oriented simulation software "Plant SimulationTM" is employed to develop the semiconductor capacity analysis and planning simulation (CPAS) system in which all the aforementioned production characteristics and constraints may be modeled by using Plant Simulation's basic elements and Simtalk programming language.

Figure 8 illustrates the implementation of a specific machine tool group's simulation model in which all the required data will be imported using ODBC and Excel, all the production constraints and dispatching rules are implemented with Method, then, Event controller will control system execution time, and Trigger will trigger events and loads data into Table File based on simulation time. Furthermore, machine tool will operate according to the logic implemented in its corresponding Method, and production time will be exported from run sheet through ODBC.

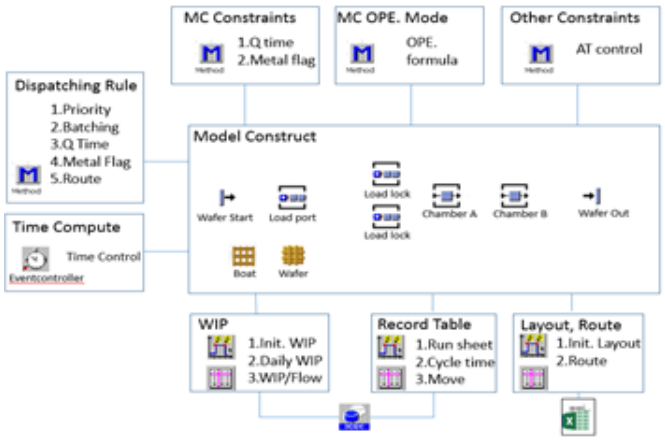

Figure. 8: A specific machine tool group's simulation model using Plant Simulation

Since CPAS is an object-oriented semiconductor wafer fab simulation model, the internal behavior of complicated machine is model as method, the pseudo code of the operation logic of single-chamber machine and multi-chamber machine are listed as follows for reader's reference:

(1) Single chamber machine

Taking the ion implanter as an example, it has three load_ports, two load_locks, two robots, and one chamber, the pseudo code of the internal behavior (i.e., operation) of this single chamber machine is listed in Table 1.

Table 1:The pseudo code of the operation of a single chamber machine

```
Procedure: Single chamber operation
    Set Cassette(C)
    Set Wafer= (W)
    Set Load port lead time (LT)
    Set Right load lock process time (LP)
    Set Chamber process time (PT)
    Set left load lock process time (DL)
      If Chamber=empty
      {
      C move into Load port and process in (LT)
      W move into Load Lock in (LP)
      W Move into Chamber and process in (PT)
      W move back to C
      Wait for DL and leave.
      }
```

(2) Multi-chamber machine

We may employ the metal etch systems depicted in Fig. 4 as an example, it has two load_ports, two load_locks (e.g., A, B), one robot, and four chambers (e.g., 1, 2, 3, 4), the pseudo code of the operations of this multi-chamber machine is listed in Table 2.

Table 2:The pseudo code of the operation of a multi-chamber machine

```
Procedure: Multi chamber operation
    Set Cassette(C)
    Set Wafer (W)
    Set Wafer Recipe(WR)
    Set wafer flag(WF)
    Set Recipe (R i) // i = recipe table row
    Set Flag (F i)// i = recipe table row
    Set Chamber(CB i)// i = recipe table row
    Set Load port lead time (LT i)
    Set Right load lock process time (LP i)
    Set Chamber process time (PT i)
    Set left load lock process time (DL i)
      If Chamber=empty
      {
          for all Recipe(R i) in this Tool
          [
          If  R i = WR and F i = WF
          C move into Load port and process in (LT i
          W move into Load Lock in (LP i)
          W Move into (CB i) and process in (PT i)
          W move back to C
          Wait for DL and leave.
          Exit for loop
      }
```

4. APPLICATIONS OF CPAS MODEL IN SEMICONDUCTOR FAB

In this section, we will illustrate the application of CPAS model in a full-scale 300 mm wafer fab in Taiwan. The accuracy of the CPAS model is validated with the actual input (e.g., wafer release per day, machine run time/available time, routing, WIP) and output (e.g., cycle time, MOVE, Wafer Out) for all machine tool sets.

Nine critical "key" machine tool groups are selected to experiment and obtain the best combination of dispatching rules assigned to these critical machine tool groups (*CMrule*) under certain practical available time (AT) and its fluctuation patterns. The numerical experiment is designed by considering three factors: (1) the average AT, (2) the machine down time pattern, (3) the dispatching rule. The base case is set as the average AT=91.64% and last for two months, the consecutive down time is 2.5 days and occurred at the beginning of the first month. Each test scenario will follow the same setting as base case except that average AT% and downtime will be reduced, that is, the average AT and consecutive downtime of scenario 1, 2, 3, and 4 are 86.64%, 81.64%, 76.64%, 71.64% and 4 days, 5.5 days, 7 days, 8.5 days, respectively. For each test scenario, four dispatching rules (i.e., FIFO, SPT, LPT, and SPRT) may be applied to nine "key" machine tool groups and the comparison of the system throughput (i.e., wafer out) between distinct dispatching rules and *CMrule* is shown in Table 5. We can obviously observe that *CMrule* outperforms the distinct dispatching rules. Take scenario 2 as example, if FIFO dispatching rule is applied for all "key" machine tools in scenario 2, only 34150 wafers may be produced in two months which is 6.76% short compared to *CMrule's* 36625 wafers. Fig. 9 illustrates partial operations schedule Gantt chart obtained by CPAS system.

Table 5: The comparison of wafer output

	CMrule	FIFO		SPT	
		WO	Diff	WO	Diff
Scenario 2	36625	34150	-6.76%	34725	-5.19%
Scenario 3	35650	33550	-5.89%	33850	-5.05%
Scenario 4	32900	32750	-0.46%	31300	-4.86%
		LPT		SPRT	
		WO	Diff	WO	Diff
		33400	-8.80%	33550	-8.40%
		32250	-11.71%	31575	-12.34%
		31475	-1.98%	31250	-4.03%

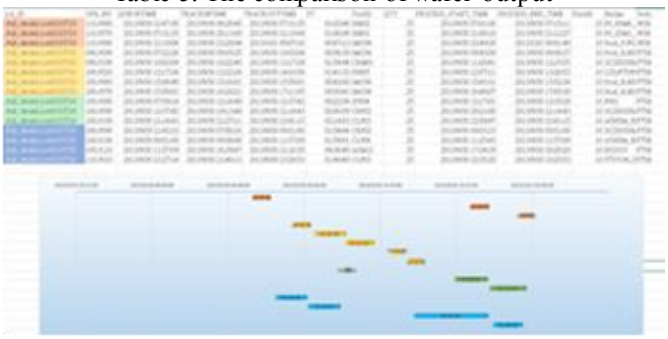

Figure 9: Partial operations schedule Gantt chart obtained by CPAS system

5. CONCLUSIONS

This paper develops a capacity analysis and plannin g simulation (CPAS) model which takes into account the production characteristics/constraints, the internal behavio r of machines, and the dispatching rules applied in a wa fer fab. CPAS model may be employed by capacity plan ners to study the impact of the available time (AT) and its fluctuation of critical "key" machine tool groups to f ab's overall capacity and throughput performance. The a pplication of CPAS model in a leading fullscale 300 m m wafer fab in Taiwan shows that the fluctuation of AT does affect throughput performance at the situation of l ong down time situation. Therefore, shop floor managers only need to watch attentively on the "key" machine too ls, which will cause high impact on the throughput, and keep their promised AT level or increase AT level. Num erical evaluation shows that dispatching rules employed by critical machine tool did affect the system performan ce (e.g., wafer out), and capacity planners may employ CPAS system to generate high quality production schedu le. For future's research, we will integrate some search algorithm (e.g., GA) with CPAS to generate the best co mbination of dispatching rules for each different manufac turing environment.

REFERENCES

Gupta AK, Sivakumar AI (2006) Job shop sched-uling techniques in semiconductor manufacturing. Int J Adv Manuf Technol 27(11):1163-1169

Bahaji N, Kuhl ME (2008) A simulation study of new multi-objective composite dispatching rules, CONWIP, and push lot release in semiconductor fabrication. International Journal of Production Research 46(14):3801-3824

Liu J, Yang F, Wan H, Fowler JW (2011) Capacity planning through queueing analysis and simula-tion-based statistical methods: a case study for semiconductor wafer fabs. Int J Production Re-search 49(15): 4573-4591

Negahban A, Smith JS (2014) Simulation for manufacturing system design and operation: Lit-erature review and analysis. J of Manufacturing Systems, 33(2):241-261

Aybar M, Potti K, LeBaron T (2002) Modeling methodology: using simulation to understand ca-pacity's constraints and improve efficiency on process tools. Proceedings of the 34th conference on Winter simulation: 1431-1435

Lin JT, Wang FK, Wu CK (2003) Simulation anal-ysis of the connecting transport AMHS in a wafer fab". IEEE Transactions on Semiconductor Man-ufacturing16(3):555-564

Lin JT, Huang CJ (2014) A simulation-based op-timization approach for a semiconductor photo-bay with automated material handling system. Simulation Modeling Practice and Theory 46:76-100

Hung MH, Wang E, Wang I (2002) Using simula-tion and daily-demand method to analyze the capacity utilization for product-mix in semicon-ductor fabrication. Int Semiconductor Manufac-turing Technology Workshop:302-306

Hubl A, Jodlbauer H, Altendorfer K (2013) Influ-ence of dispatching rules on average production lead time for multi-stage production systems. Int. J. Production Economics 144:479-484

Chao Q, Sivakumar AI, Gershwin SB (2008) Im-pact of production control and system factors in semiconductor wafer fabrication. IEEE Transac-tions on Semiconductor Manufacturing 21(3):376-389

Nazzal D, Mollaghasemi M, Anderson D (2006) A simulation-based evaluation of the cost of cycle time reduction in Agere systems wafer fabrication facility—a case study. Int J Production Economics 100(2):300-313

Thiesse F, Fleisch E (2008) On the value of loca-tion information to lot scheduling in complex manufacturing processes. Int J of Production Economics, 112(2):532-547

OMG (2001) Model Driven Architecture, http://www.omg.org

Jain AK, Murty MN, Flynn PJ (1999) Data, clus-tering: a review. ACM Computing Survey 3(3):264–323

Chien CF, Wang WC, Chen JC (2007) Data mining for yield enhancement in semiconductor manu-facturing and an empirical study. Expert Systems with Applications 33:192-198

Chien CF, Hsu CY, Hsiao CW (2012) Manufac-turing intelligence to forecast and reduce semi-conductor cycle time. J Intell Manuf 23:2281-2294