WIP Management Systems for BullWIP Management in Semiconductor Fabrication Foundry

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Abstract. Complementary Metal Oxide Semiconductor (CMOS) is a complex and very delicate process in semiconductor. In typical 30,000 wafer capacity of single foundry business model, the CMOS product loads are mixed from various technologies to serve wider market segments. At similar time frame, total devices loading with difference processes steps and cycle time can be loaded up to 200. This approach creates variables for process time, equipment usage, number of processing steps which leads to inconsistent WIP profiling at respective time period which finally leads to BullWIP situation. In this paper, the approach to maximize the output is used by changing the methodology of WIP movement through a good WIP Profile chart management. An optimize WIP management approached can improve the FAB out at least by 5%. It will also help the factory to make a right decision to manage the WIP balancing especially when we face BullWIP situation. The Production Control will get a good benefit from this study. A linear plan is no longer work in managing BullWIP situation and an approach on how to improve the line balancing is required.

Keywords: Day per Mask Layer (DPML), Work In Progress (WIP), WIP profile, CMOS, Foundry

1. INTRODUCTION

Semiconductor manufacturing is the most complex manufacturing process in the world(Ibrahim, Chik, & Hashim, 2014). The semiconductor manufacturing is a multistage process which transfers silicon in the form of thin, polished wafer into integrated circuits(Bates, 2000) . The entire process basically includes four main steps: Raw wafer manufacturing, wafer fabrication, probe and die, package and test(Bates, 2000; Qi, Sivakumar, & Gershwin, 2008). The wafer fabrication is most time-consuming and complicated one, consisting primarily of at least six major types of phases or module: Diffusion, Lithography, CVD, Thin Film, Etching and Ion Implantation(Mohd Azizi Chik, Yeo, & Lim, 2002; Leachman, Ding, & Chien, 2007). The wafers pass the through these six major modules numerous times (Bates, 2000). The cycle time of a wafer is typically 45 to 60 days. The entire fabrication process involves hundreds of operation steps performed on a variety of machines and Wafers are grouped in lots and transferred in a standard cassette(Qi et al., 2008). A wafer must visit some machine groups more than once. The process is typically reentrants process through many resources(Pfund, H, Fowler, Mason, & Rose, 2008).

For instance, a wafer may have to visit the photolitoghraphy module 20 to 38 times for all layers of circuitry to be fabricated. This complexity of the wafer fabrication process caused wafer release and dispatching

decisions are extremely difficult to be achieved (Leachman, Kang, & Lin, 2002; T Krisnamuthi, MA Chik, TT Ung, KW Lim, 2012). It results to poor cycle time if the dispatch is not optimized(Chang, Su, & Chen, 2008).

The maximization of critical resource utilization as well as throughput rate and the minimization of cycle time are the primary goals of the release and dispatching policy in wafer fabrication because of its capital-intensive nature and the need to attain a competitive advantage(Leachman et al., 2002). Wafers generally move through in lots in a wafer fabrication factory. The operational batch sizes range from a single wafer to several lots(Ibrahim, Chik, Sharnsir, Fern, & Za'bah, 2003). Processing times depend mainly on the operation types. For a single wafer processing tools like photolitoghraphy, the processing time depends on the number of wafers in a lot. For batch processing operations like Diffusion, no matter how many lots are loaded at a time (the number of lots batched must be smaller than the maximal batch size which is usually 6 lots or 150 wafers), the processing time generally does not vary with the number of lots batched(Ibrahim et al., 2003).

There are many characteristics of wafer fab like in Fig. 2, such as re-entrance processing flow, batch tools, inter related and dependent process sequence, unpredictable equipment failure and so on, which differentiate wafer fab from other traditional flow shop or job shop(Chang et al., 2008; Chen & Boylan, 2009). Normally, release strategy and dispatching strategy are two major ways which are applied to control the wafer fab with the purpose of decreasing average cycle time and cycle time variance, achieving on time delivery of the products(Chang et al., 2008; Huang & Yuan, 2010; Karmarkar, 1989; Muhammad, Chin, Kamarrudin, Chik, & Prakash, 2015). Many methods were used on applying the dispatching strategy to wafer fab.

There is strong correlation between cycle time and the factory utilization(Chen & Boylan, 2009; Mohd Azizi Chik, Yung, et al., 2010; David, 2011). As the utilization increase, the cycle time may deteriorate. With the WIP increase, the queue time to process will also increase. Due to the delicate semiconductor process, the high queue time to process will increase respective process especially at higher reentrance level. Cycle time in wafer fabrication is measured by day per mask layer (dpml). It is a method to measure the reentrances at lithography process. Day Per Mask Layers is an indices in wafer fabrication industry to monitor the cycle time (CT) or Turn Around Time (TAT)(Mohd Azizi Chik et al., 2012; SICAS, 2011). It is measuring by the average of the mask layers being processed during the fabrication step. Mask is the circuitry design to print on the wafers during the fabrication process. It has multi layers during the lithography or stepper process.

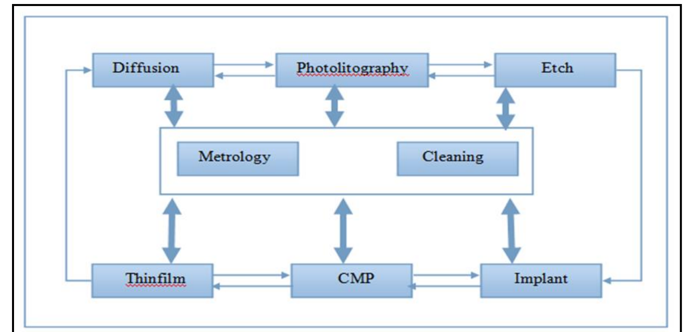

Figure 1: Typical Wafer Fabrication Process

BullWIP situation happens when there is high WIP at a particular step or process. The BullWIP can happen due to :

1) High WIP at bottleneck (BN) areas.
2) Poor process or tools performance
3) Poor BN Management.
4) Over capacity. Load above capacity.

Although the bottleneck is the most critical work center which determines the performance of the whole fab, feeding empty non-bottleneck work centers can also smooth the material flow, avoid capacity losses of machines, and improve product cycle times (Barahona, Bermon, Günlük, & Hood, 2005; Bermon & Hood, 2009). Therefore, a minimum workload 1.5 hours is also defined for the non-bottleneck work centers. If the workload of non-bottlenecks drop to this minimum workload level, lots are scheduled to feed it to avoid starvation(Mohd Azizi Chik et al., 2002).

Production Control (PC) will assign the layers output for each process. Production Control main function is to ensure the On Time Delivery (OTD) for each device and orders quantity for each customer is met. Production Control has the privilege to upgrade and downgrade the lots to ensure the OTD are protected. At the same time PC will also has the function to control the WIP movement. PC will apply the Line Balancing concept to maximize the moves and utilization by applying Starvation Avoidance concept to ensure there is no resources are idle. PC function as FAB planners are very critical and important to make sure the resources are busy and moving the right WIP. PC will be responsible for the resources' daily planning move and output.

In typical Integrated Module (IM) activity, PC will assign moves or output for each IM based on the resource capacity and the capability to the IM to produce the moves or the output. Due to the re-entrants process, PC will assign a balancing target moves or output for each layers. The plan is done through manual calculation and it will be uploaded to the system to track the moves and the output. A report to monitor the output hourly will be automated through email

and the reporting system to ensure the right layers and moves or output achieved.

The Line Balancing concept is important and by developing the WIP Profile report, it will help the PC and Manufacturing Manager to manage the WIP movement. Since the processes are re-entrants, any spike WIP in the WIP Profile show the real time issue face by the line. It can be due to tools downtime, or WIP congested due to capacity constraint (Taha, 2010). Applying Bottleneck Management (BN) concept or Theory of Constraint (TOC) is deem needed to ensure the BN resources which determine the FAB capacity are fully loaded with WIP (Shanthikumar, Ding, Zhang, & Member, 2007). At the same time it is also important to avoid high WIP waiting at the BN resources. The PC function is important to avoid the WIP pile up and queue in front of the BN resources by moving the WIP to resources that starving or idle(Mohd Azizi Chik et al., 2002).

2. METHODOLOGY

In order to optimize the WIP management strategy we need to develop systems that able to provide critical information and also a system that's able to implement into the production line.

Darlington, Francis, Found, & Thomas, (2014) proposed selected longitudinal case study conducted over 24 months and organized around a two phase research design which includes numerous unstructured interviews and observation of shop floor practices; document and archival analysis, and 140 photographs of the focal operation. Information related to financial and operational data extracted from the firm's accounting and MRP systems to construct and implement bespoke capacity planning, work in progress (WIP) monitoring and simulation modelling tools.

Zhang, Jiang, & Chengtao, (2009) proposed Dynamic Bottleneck Dispatching (DBR) method to improve the Line Balancing and Real time dispatching by prioritization in the system. The study consist of the Offline and Online module with all the parameters used for the dispatching to work and also from the equipment schedule based on the plan preventive maintenance (PM) or unplanned maintenance (UM), WIP situation at the downstream etc.

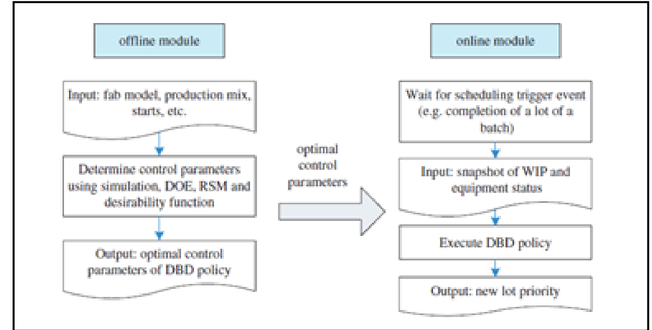

Figure 2: Overview of the system scheduling architecture by Zhang et al (2009).

The purpose of this study is to supplement Zhang et al (2009) proposal so that we have more visible line monitoring.

2.1 Developing a Dispatching System

In developing a line balancing monitoring, we have to review the overall factory WIP. A profile of WIP distribution to indicate the inventory level of each steps or stages will help the Production Control (PC) and Factory Manager (FM) to manage the production floor effectively. The facts that a resource has to run multiple layers or the process re-entrant to the tools need a very systematic approach both in the dispatching system as well as the output plan. Figure 3 shows how the MES link to a few servers to create a dispatching system that will have to enable the operators to plan their lots sequencing and loading. With the help from CIM and Manufacturing System Engineers, a good dispatch system was established. The global and local rules are implemented to ensure the On Time Delivery and optimizing the factory revenues with a good BN management is in place.

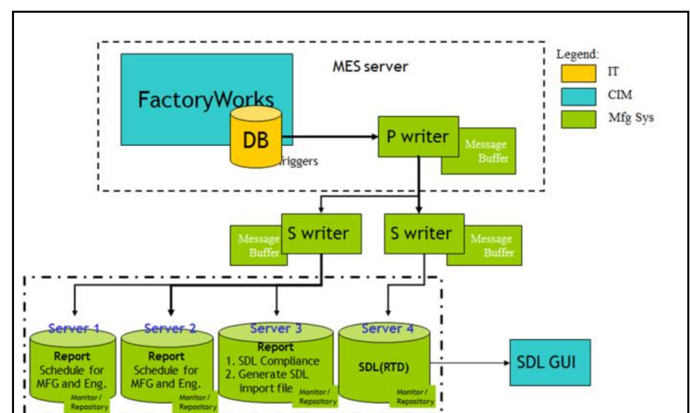

Figure 3: Integrated Dispatching Systems

A global rule is set in the factory dispatching rules. It will govern the factory wide lot movements by:

1) Lot Priority
2) Shipment due date.
3) Starvation Avoidance for BN area.
4) Critical Ratio

Above are parts of global rule used to determine the overall factory dispatching system. But for each individual areas and resources, there is local rules allowed to maximize the output of the equipment and the factory.

Local rules consist of:

a) Running in a batch
b) Running same recipe
c) Based on species when it is related to the life the

A dispatch system that build in the factory is required to ensure standardization since information cascade to the production floor will not be same page to deliver important instruction from top to operators (Mohd Azizi Chik et al., 2002). The data then summarized to provide information on incoming WIP or next area WIP, recipe release, tool process preferred to run (yield, cost) and issue at next step. Others information includes information needed to batch PRD and test wafer together for optimum output and move.

Literature shows that dispatching rules can be measured. The measurement of compliances of the dispatching rule follow the similar concept by M A Chik, Ahmad, & Jamaluddin, (2004).

2.2 Developing a WIP Profile Management

Manufacturing Execution System (MES) mainly used to manage WIP and equipment automation in the FAB (Mohd Azizi Chik, Ung, et al., 2010). Huge amount of data are recorded automatically in multiple databases during fabrication process where the data become the input to monitor lot movements in the semiconductor fabrication plant, or shortly FAB. MES database composed of a collection of sub systems, each with a specific task contributes to huge database because every single transaction needs to be recorded.

In Fig.3, the WIP Profile has been designed using the concept of small data warehouse by understanding and analyzing the business needs in this FAB. Based on the current framework and the application layout, the report generator architecture has been constructed using the concept of top down view as shown in Fig. 3 below. This approach will select only the relevant information needed for faster data retrieval and accuracy.

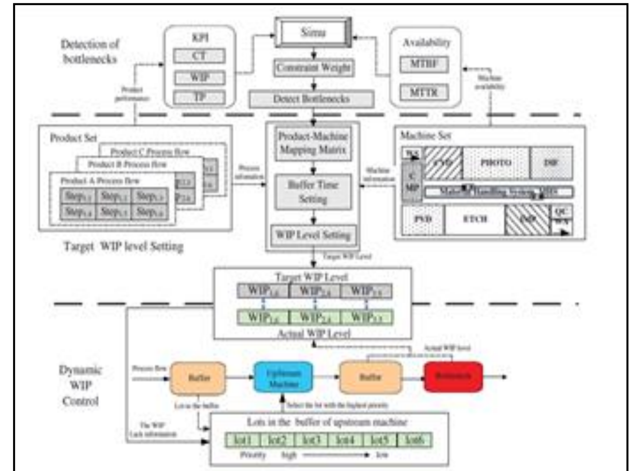

Figure 4: Integrated Dispatching Systems

The data retrieves mainly from MES application to get the WIP, movement and process flow information. This data will be consolidating with other external application that is 90% of the information is extracted from APF repository data. In addition, external custom data from the user also will be used for this process. Data from multiple databases will be on cleansing, de-duplication and transformation to more reliable and meaningful data. In this design, the query approach has been used to summarize the data and it will be store into a data mart. Materialized view concepts also have been used for efficient data retrieval. Materialized views have been found to be very effective in speeding up query as well as update processing. A few server have been schedule to run the automated jobs to generate the summarize data. Users are able to view this information through web page, Reporting System or even email.

Production Control (PC) will use a layer plan system to determine number of moves required for each layers and will map with the resources capability to meet the plan output or moves. The layers plan system will use the wafer per hour (WPH), equipment availability and utilization from the Industrial Engineering data base (IEDB) to match the moves requirement. In the case of BN area, maximizing the moves will help to optimize the factory output. A close monitoring moves plan requirement is set by the PC.

3. BULL WIP MANAGEMENT

Fig. 5 illustrated WIP profile for BullWIP situation

Based on the Fig. 5, BullWIP area is at middle process of wafer fabrication or salicide process module. Daily capacity for salicide is 1200, with sufficient WIP, PC will plan 1200 move. There are incoming WIP to this stage. The incoming WIP is based on completion of 3 stages, or turns (TR), a day. Therefore in this example, its means in one day

there WIP total from 3 stages forecasted to arrive to salicide.

Figure 5: WIP profile

PC will plan the incoming and projected Salicide WIP after 5 day. Salicide currently have 6960 WIP in front of the tool, there are 825 WIP expected will come to this stage in same day, called incoming WIP to Salicide Day1.Based on the projected incoming WIP, and daily move 1200 out from Salicide, after 5 days the WIP will drop from 6960 to 5448. Fig 6 shows how PC put the plan to ensure better line balancing. The overall plan and schedule for the Bull WIP area will help to linearize the FAB line balancing. PC will maximizing the moves and at the same time will look at the incoming WIP to predict the final WIP after 5 days. Even though there is potential reduction a longer plan is required to see the potential WIP reduction at the Bull WIP area. During this time PC will work closely with Manufacturing System team to simulate the moves and also ensure the local rules dispatching system is being set to meet the PC plan moves without jeopardize the delivery.

	Incoming WIP	STAGE	EOH	PC Plan
Incoming to Salicide Day5		GA_SpcNEth	350	900
		GA_NSDMask	350	900
	979	GA_NSD-Im	279	950
Incoming to Salicide Day4		GA_NSDImRS	289	950
		GA_PSDMask	398	950
	987	GA_PSD-Im	300	950
Incoming to Salicide Day3		GA_PSD-ImL	100	900
		GA_PSDImRS	406	800
	956	GA_TEOSBlk	450	950
Incoming to Salicide Day2		GA_LTOBlck	162	400
		GA_SDAnRTP	304	900
	741	GA_SINBlck	275	750
Incoming to Salicide Day1		GA_BlckMsk	300	900
		GA_BlckEtc	350	925
	825	GA_BlockRS	175	925
		GA_Salicid	6960	1200

GA_Salicid

	BOH	Incoming	Plan Move	EOH
Day 1	6960	825	1200	6585
Day 2	6585	741	1200	6126
Day 3	6126	956	1200	5882
Day 4	5882	987	1200	5669
Day 5	5669	979	1200	5448

*Incoming is based on 3TR,means 3 stages incoming WIP apart from GA_Salicid daily

Salicide Day1	825	GA_BlckEtc	350	925
		GA_BlockRS	175	925
		GA_Salicid	6960	1200

*Incoming is based on 3TR,means 3 stages incoming WIP apart from GA_Salicid daily

Figure 6: Illustration of PC plan table

$$TR_z = \frac{\frac{1}{m}\sum_{j=1}^{m}\sum_{i=1}^{n} Stage_i}{CycleTime_z} \qquad (1)$$

$$\sum_{Proj}^{i} WIP = \sum_{curr}^{w} WIP - \sum_{di-d5}^{m} Moves + \sum_{d1-d5}^{w} WIP \qquad (2)$$

$$\sum_{d1-d5}^{m} Moves = \sum_{d1}^{m} Moves + \sum_{d2}^{m} Moves + \sum_{d3}^{m} Moves + \sum_{d4}^{m} Moves + \sum_{d5}^{m} Moves \qquad (3)$$

$$\sum_{d1-d5}^{W} WIP = \sum_{d1}^{W} WIP + \sum_{d2}^{W} WIP + \sum_{d3}^{W} WIP + \sum_{d4}^{W} WIP + \sum_{d5}^{W} WIP \qquad (4)$$

TR = Turn Ratio

w = WIP

m = Moves

proj = projection WIP

curr = current WIP

d1-d5 = day1 to day5

(1) TR calculation

(2) WIP projection calculation

(3) Daily Moves projection for Day1 to Day5

(4) Incoming WIP projection for Day1 to Day5

Moves plan based on TR calculation. And for each of the projection in Fig 7, PC will use above formula calculation to plan and forecast moves and WIP. Moves summary is from PC moves plan calculation, an assignable TR is being set to each stage and with the capacity allocation given to each stages. The move is planned for the Manufacturing team to meet and a layer plan moves rules also applied in the dispatching rules to govern the operators on right lots selection.

The rules of PC plan moves will help to maximize the moves and also repairing the line balancing by focusing additional moves requirement at a Bull WIP areas like Fig 6.It will definitely improve the factory output and delivering the WIP to downstream process is very delicate process that required a diligent planning.

In any case of BullWIP situation PC will increase the

requirement of moves. Typically for 30,000 per month fab out capacity, the Salicide moves requirement is ~ 1000 moves/day. Due to the BullWIP issue, PC increase the moves requirement to 1200 moves/day anticipating that the BullWIP will be reduced in 3 weeks by having extra 200 moves more per day. Based on the incoming WIP ~ 1000 per day, the Salicide WIP will reduce to 2365. The ideal WIP for Salicide Dep stages is ~ 2200 wafers due to the multiple steps process for this stage. The Salicide Dep stage consists of 6 process steps.

At the same time to ensure the On Time Delivery intact, an assignable rules of due date has to be respected as well. It must be one of the global rules in the Dispatching System that must be executed well. The layer plan will help to ensure the focus given linearly and well balancing for the resources to run each layers.

Typically a product will go through ~ 32 layers at Photolithography. Depending on the geometry of the Critical Dimensions (CD) to be printed, the Photolithography steps are mainly for Iline and DUV scanners. The critical layers (Lower geometry < 300 nm CD) are printed at DUV. The noncritical layers will be printed at Iline (> 300 nm CD).

Looking at the capacity and requirement of moves, which typically will be aligned with the wafer loading pattern, PC team will be allocating the layers moves at each resources. In Table 1; is a typical layer plan for a multiple reentrants process and steps at photolithography.

This is the daily plan done by the PC team to linear the moves requirement in order to ensure the line balancing intact. A required layer plan moves is being planned by the PC based on the wafer start loading volume and it must match with the capacity. PC will set the target daily and at linear phase. There is an increment of moves requirement in any case of BullWIP situation happen. The dynamic plan has to do together with the Manufacturing System so that the Dispatching system will assign the right lots and layers. The target moves will be set in the Dispatching List. If the moves of the particular layers are met, the system will assign more lots to the next layers depending on the moves delta.

Table1: A typical PC layers plan for Photolithography Steps

Date	Module	IE_RESOURCE	Step	Move_req	Act_Move	Delta_move	EOH
4/28/2016	PHO	PHO-ILINE	NWell-Mask-CED	600	600	0	175
4/28/2016	PHO	PHO-ILINE	PWell-Mask-CED	600	750	150	325
4/28/2016	PHO	PHO-ILINE	HRPoly-Mask-CED	600	450	-150	100
4/28/2016	PHO	PHO-ILINE	NLDD-Thick-Mask-CED	600	1125	525	354
4/28/2016	PHO	PHO-ILINE	PLDD-Thick-Mask-CED	600	952	352	275
4/28/2016	PHO	PHO-ILINE	NSD-Mask-CED	600	871	271	300
4/28/2016	PHO	PHO-ILINE	PSD-Mask-CED	600	871	271	102
4/28/2016	PHO	PHO-ILINE	Block-Mask-CED	600	575	-25	250
4/28/2016	PHO	PHO-ILINE	MIM2_5-Cap-Mask-CED	600	575	-25	172
4/28/2016	PHO	PHO-ILINE	TopMet-Mask-CED-HS	600	827	227	411
4/28/2016	PHO	PHO-ILINE	Pad-Mask-CED	600	964	364	353

PC will further monitor the moves requirment to ensure the average moves in a particular months are met. The dynamic activity in the wafer fabrication due to multiple pull in shipment requirement, equipment down for maintenance, WIP movement issue due to upstream constraint, BN performance issue, Customer hold etc will cause imbalance WIP movement that may impact the daily moves plan. The dynamic moves plan by PC will help to reduce the gap in any specific layers loss. At the end of each month, monitoring on the average layers move is necessary to improve the gap loss and ensure the gap is closer.

At the same time the Manufacturing System Engineers will work on the right methodology to determine the best dispatching method to ensure a proper layer plans for each steps. The combination of the layer plans given by the PC , BN management and Due Date for each lots and device will automate the lots sequencing for the operators. It will improve the factory utilization and increase the factory output.

The dispatching system will also improve to optimize a good batching system and it will benefit a good cascading to run the process and equipment. In order to monitor the WIP balancing, PC will assign layers plan move to each areas and process.

The FAB WIP is divided to seven different segmentations. It will make the plan more systematic which also illustrated in Fig 4.

1. Pre Poly 1 - From Wafer dispatch to STI Anneal
2. Pre Poly 2 - From HNwell Mask to PWell Anneal RTP
3. Poly - From MVGate Pre Clean to Poly Etch
4. Post Poly 1 - From Poly ReOx Pre Clean to Spacer Nitride Etch Resist Strip
5. Post Poly 2 - From NSD Mask to ILD CMP
6. Backend - From Contact Mask to Top IMD CMP.
7. Final - From Top Via Mask to Outgoing Quality Inspection

4. CONCLUSION AND SUMMARY

Earlier studies shows literature on WIP management to ensure bottleneck is not idle through capacity planning, continuous expansion, starts plan optimization and also dispatching systems (C. F. Chien, Chen, & Peng, 2010; C.-F. Chien, Hsu, & Chang, 2013; M A Chik et al., 2004; Ibrahim & Chik, 2010; Karmarkar, 1989; TSMC, 2010, 2014)This paper further enhances the dispatching implementation strategy to more comprehensive scopes including reporting systems strategy using real 200mm wafer fab case study.

Developing an automated WIP Profile monitoring

benefits for the PC and Manufacturing team to monitor the WIP movement real time. The nature of the process and technology in the wafer Fab that process more than 200 devices with different volume at any time, the linear start is not necessary will be a linear output. And it will also not necessary a linear line balancing. It required a close WIP monitoring and having the real time automated WIP Profile report will benefit the PC and Manufacturing team to fine tune the WIP and also the dispatching rules.

Managing the BullWIP and allocating the required output for each process especially that having multiple reentrants process like Photolitography, Etch Implanters are very important for Production Control. They will ensure the Manufacturing team execute the right layers and step also not to overdo on certain steps to avoid Bottleneck tool from starving. Thus having the automated WIP profile report will definitely advantages for FAB WIP WIP management systems will bring in more revenue and output for the company.

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